REMARKS/ARGUMENTS

Claims 1 and 3-31 were previously pending in this application. Claims 1 and 3-25 were rejected and claims 26-31 withdrawn from consideration. Claims 1, 8 and 15 are hereby amended and claim 5 cancelled.

Applicants respectfully request re-examination, reconsideration and allowance of each of presently pending claims 1, 3, 4 and 6-25.

Applicants respectfully submit that the claim amendments leave the application in allowable form and therefore respectfully request entry of the claim amendments.

I. Rejection of Claims 1 and 3-25 Under 35 U.S.C. § 103

On page 2, fourth paragraph of the Office Action, claims 1 and 3-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Noda (USPN 6,512,299 D1) in view of Bryant et al (USPN 6,436,744 B1), hereinafter "Bryant". Applicants respectfully submit that each of these claim rejections is overcome for reasons set forth below.

Independent claim 1 recites the feature of:

> the active region serves as a local connection layer between the first and second semiconductor devices.

This feature is shown in FIG. 3 of the originally-filed specification and previously appeared in claim 5, now cancelled. Noda, in contrast, does not disclose or suggest using the active region for providing connection between multiple devices. Rather, the encroaching silicide layers 23 or 64 of Noda only connect a gate electrode *of one semiconductor device* to an adjacent active area from which it is otherwise separated by a dielectric. Neither Noda nor Bryant disclose the feature of the active region connecting multiple devices as is recited in claim 1. Claim 1, and therefore also dependent claims 3, 4 and 6-7 are further distinguished from Noda in view of Bryant.

Claim 1, and therefore also claims 3, 4, 6 and 7 which depend from claim 1, are distinguished from the references of record and the rejection of these claims should be withdrawn.

On page 4, fourth paragraph, the Office Action rejects claims 8-25 under 35 U.S.C. § 103(a) as being unpatentable over Noda in view of Bryant and further in view of Sundaresan (USPN 5,298,782). Applicants respectfully submit that each of these claim rejections is overcome for reasons set forth below.

Each of the independent claims of the rejected claim set, i.e., claims 8 and 15, recite the feature that a silicide layer serves as an intra-cell connection layer connecting drain nodes of at least one PMOS transistor and an NMOS transistor formed on an insulator substrate and also connecting source/drain regions to transistor gates. In particular, independent claim 8 recites the feature of:

> at least one active region formed on the insulator substrate and with a continuous silicide layer formed thereon serving as an intra-cell connection layer connecting drain nodes of at least a PMOS transistor and an NMOS transistor formed on the insulator substrate, the two transistors forming a first inverter; and
>
> said continuous silicide layer further forming a sidewall butted connection structure used in conjunction with a gate interconnect layer and connecting the drain nodes of the transistors of the first inverter to gates of at least two transistors of a second inverter.

Similarly, amended independent claim 15 recites the feature of:

> a *sidewall butted connection structure used in conjunction with a gate interconnect layer for connecting drain nodes of the transistors of the first inverter formed on an active region disposed on the insulator substrate, to gates of the two transistors of the second inverter*; and
>
> wherein *the sidewall butted connection structure is a continuous silicide layer* including a junction covering a

dielectric edge portion between the active region and the gates of the two transistors.

The distinguishing feature of the continuous silicide layer connecting drain nodes of different transistors is supported in FIG. 3 of the originally-filed specification and paragraph [0027] which recites "the connection, by the silicided neck 330, between the drains 322 and 326 obviates two contacts, one to each drain, that are necessary in previous technologies. The two drains 322 and 326, connected by the silicided neck 330, form the storage node of the inverter 318". FIG. 3 further clearly shows silicided area connecting source 320, source 324 and drain 306 (corresponding to feature 210 of FIG. 2) simultaneously without additional metal wiring or dedicated contact holes. It is **because** of this miniaturization feature, that additional metal wiring and dedicated contact holes for providing connection to 320, 324 and 306, for example, is not needed. According to conventional technologies, additional metal wiring and additional contact holes are required and such features require additional space therefore increasing chip area and reducing wire routing freedom.

In particular, the Noda reference does not teach or suggest using the continuous silicide layer to connect drain nodes of PMOS and NMOS transistors, or any transistors. Bryant has been relied upon for providing an insulator substrate and does not cure the deficiencies of Noda. Independent claims 8 and 15 are therefore distinguished from the references of Noda and Bryant. Sundaresan has apparently been relied upon for providing a circuit diagram showing the wiring of an SRAM cell that includes inverter structures but FIGS. 1 and 3a-3d of Sundaresan do not provide a device layout that could accommodate a continuous silicide layer coupling the drains of separate transistors such as NMOS and PMOS transistors while also connecting drain regions to gates and Sundaresan provides no suggestion for doing so.

Since Sundaresan does not make up for the deficiencies of Noda and Bryant, claims 8 and 15 and also dependent claims 9-14 and 16-25 are therefore distinguished from the references of Noda, Bryant, and Sundaresan, taken alone or in combination.

Therefore, the rejection of independent claims 8 and 15 and of dependent claims 9-14 and 16-25 under 35 U.S.C. § 103(a) as being unpatentable over Noda in view of Bryant and further in view of Sundaresan should also be withdrawn.

Each of claims 1, 3, 4 and 6-25 is distinguished from the references of record and Applicants submit that these claims are in allowable form.

Appl. No. 10/815,201 Attorney Docket No.: N1280-00180 (TSMC2003-1083)
Reply dated: 07/20/2006
Response to Office Action of: 04/20/2006

CONCLUSION

Applicants earnestly believe that the application is now in condition for allowance and because of such, earnestly solicit the Examiner to enter the aforementioned amendments.

In particular, based on the foregoing, each of pending claims 1, 3, 4 and 6-25 is in allowable form and the application in condition for allowance, which action is respectfully and expeditiously requested.

The Assistant Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may associated with this communication, to Deposit Account 04-1679.

Respectfully submitted,

Dated: July 20, 2006

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